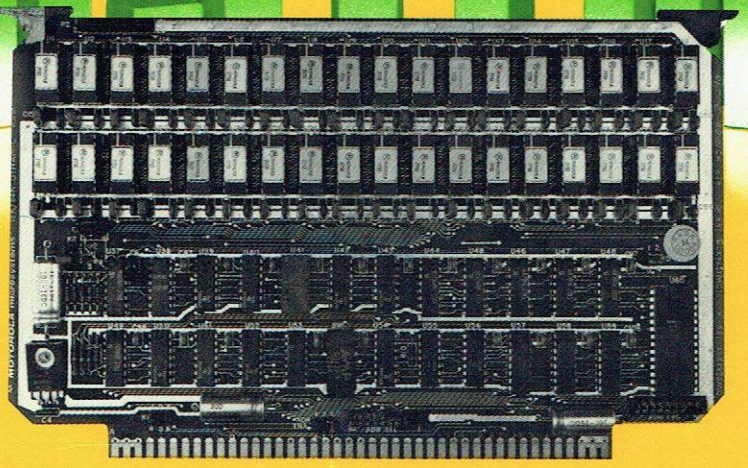
MOTOROLA

MEX6864(D)

MEX6816-22D
MEX6832-22
MEX6848-22
MEX6864-22
16K/64K DYNAMIC RAM MODULE

User's Guide

SYSTEMS



MICROSYSTEMS

MEX6864(D)
MAY 1978

MEX6816-22D
MEX6832-22
MEX6848-22
MEX6864-22

16K/64K DYNAMIC RAM USER'S GUIDE

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CHAPTER I
GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides general information, installation instructions, programming considerations, and theory of operation for the MEX6816-22D (16K), MEX6832-22 (32K), MEX6848-22 (48K), MEX6864-22 (64K) Dynamic RAM Modules. A typical module is shown 1-1. All address references within this manual are shown in hexadecimal unless otherwise indicated.

1.2 FEATURES

The features of the Dynamic RAM Module include:

- 16384 X 8 bits, 32768 X 8 bits, 49152 X 8 bits, or 65536 X 8 bits of memory organized into one memory array.
- Switch selectable base memory address on the 16K module.
- Series II DSB (Dynamic System Bus) provides Page Enable and Parity Error control.
- Enable jumpers allow module to be addressed via VUA, VXA, or Page Enable.
- Jumper selectable memory speed (1.0 MHz, 1.5 MHz, or 2.0 MHz).
- Bus drive capability.
- Even parity circuitry with jumper selectable connector outputs.
- TTL voltage compatible high impedance inputs.

1.3 SPECIFICATIONS

Dynamic RAM specifications are identified in Table 1-1.

1.4 GENERAL DESCRIPTION

The Dynamic RAM modules have a single memory array consisting of 36 Dynamic RAM devices (16K and 64K modules), 18 Dynamic RAM devices (32K module), and 27 Dynamic RAM devices (48K module). Multiple modules may be used to extend the memory capability.

A base address switch on the 16K module permits the user to select base memory addresses (0000, 4000, 8000, C000). The 32, 48 and 64K modules have a standard base of 0000. The modules refresh their memory on a system cycle stealing basis.

The module circuitry generates and detects even parity. The module outputs a parity error signal to the system whenever a parity error is detected. The output is jumper selectable to the system bus as a parity error to the system, a non-maskable interrupt, or a custom interface through the Dynamic System Bus (DSB).

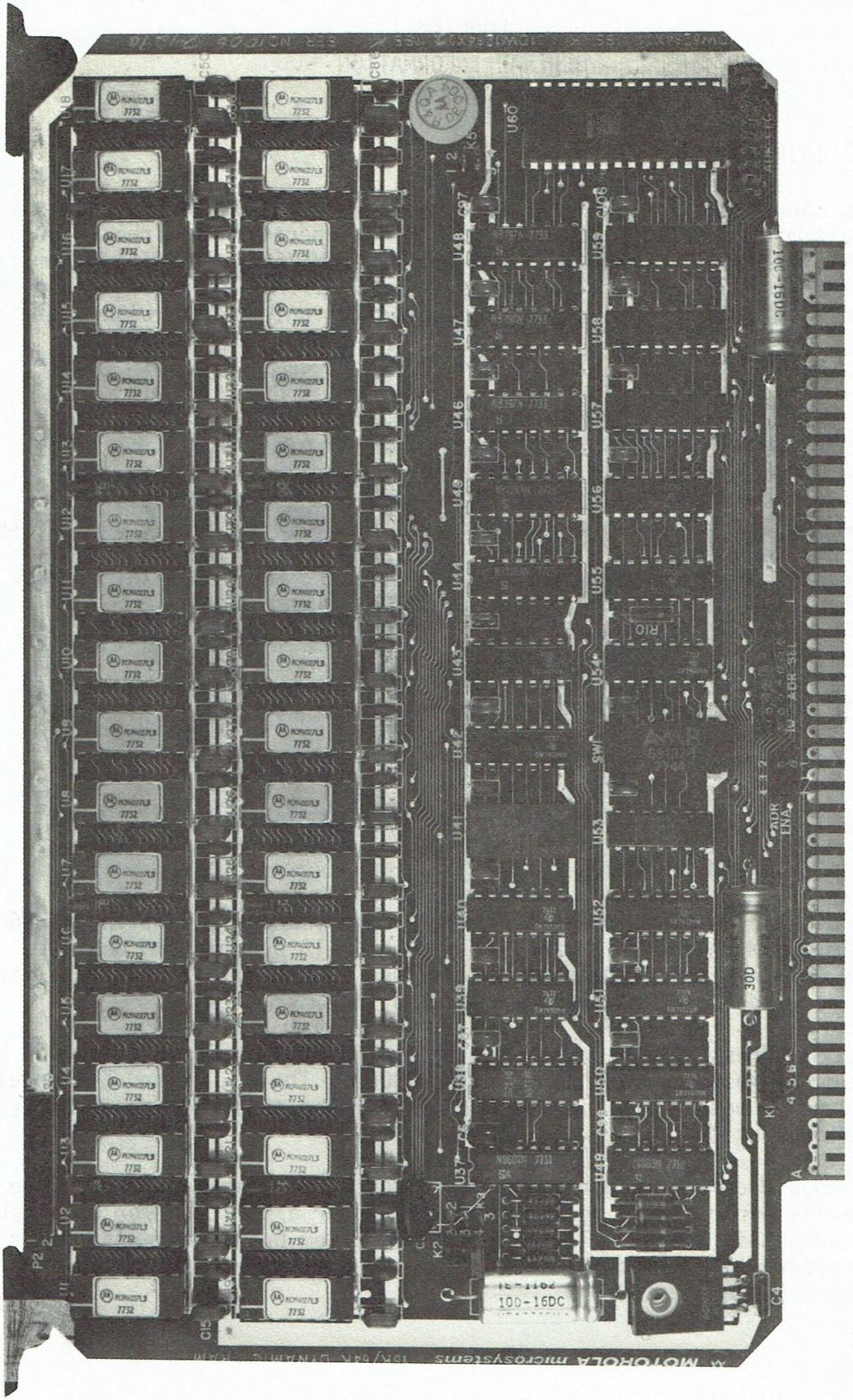


Figure 1-1. Typical Dynamic RAM Module

In the upper left-hand portion of the module is a 20-pin header, P2, known as the Dynamic System Bus (DSB). Parity error and page enable lines are connected to the DSB. The parity error and page enable lines are typically high speed lines and are, therefore, paired with a ground for twisted-pair connections.

Memory speed is jumper selectable at 1.0 MHz, 1.5 MHz, or 2.0 MHz. The user should select the speed that comes closest to his system speed.

Table 1-1 Dynamic RAM Module Specifications

Characteristic	Specification
Memory Type	MOS Dynamic RAM
Memory Organization	16,384 X 8 bits (16K), 32,768 X 8 bits (32K), 49,152 X 8 bits (48K), 65,536 X 8 bits (64K).
Parity	Even parity
Read Access Time	200ns from row address strobe (230 ns from leading edge of memory clock)
Input Signals	
Commands	TTL voltage compatible
Address	TTL voltage compatible
Data Bus	Three-state TTL voltage compatible
Operating Temperature	0^{o} to 70^{o}C
Power Requirements	+5 Vdc at 1.5A (max) +12 Vdc at 1.6A (max) -12Vdc at 110mA (max)
Dimensions	
Width and Height	9.75 inches X 6.15 inches
Board Thickness	0.062 inches

CHAPTER 2

INSTALLATION INSTRUCTIONS, PROGRAMMING AND INTERCONNECTION CONSIDERATIONS

2.1 INTRODUCTION

This chapter provides the unpacking, inspection, installation, programming and interconnection instructions for the 16K, 32K, 48K, and 64K Dynamic RAM modules. This chapter also discusses the module interconnection signals.

2.2 UNPACKING INSTRUCTIONS

Unpack the Dynamic RAM module from the shipping carton, and referring to the packing list, verify that all of the items are present. Save the packing materials for storing and reshipping the module. If the shipping carton is damaged upon receipt, request that the carriers agent be present while the module is being unpacked and inspected.

2.3 INSPECTION

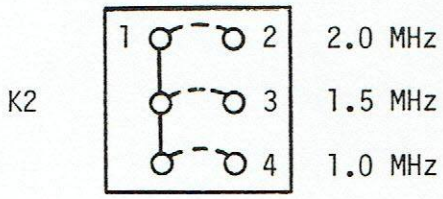
The Dynamic RAM module should be inspected upon receipt for broken, damaged, or missing parts, and physical damage to the printed circuit board.

2.4 HARDWARE PREPARATION

The 16K Dynamic RAM module is populated with 4K X 1 devices. The 32K, 48K, and 64K modules are populated with 16K X 1 devices. In each version the memory is single array organized into blocks (rows) of memory. Specific rows may be disabled or arranged in a different sequence.

2.4.1 MEMORY SPEED SELECT

The Dynamic RAM module has three over-lapping speed ranges. Depending upon the system configuration and the development requirements of the target systems, the user must select one of three clock options. Fixed clock rates of 1.0, 1.5, or 2.0 MHz may be selected. Jumper K2 is used to make this selection, as shown below.



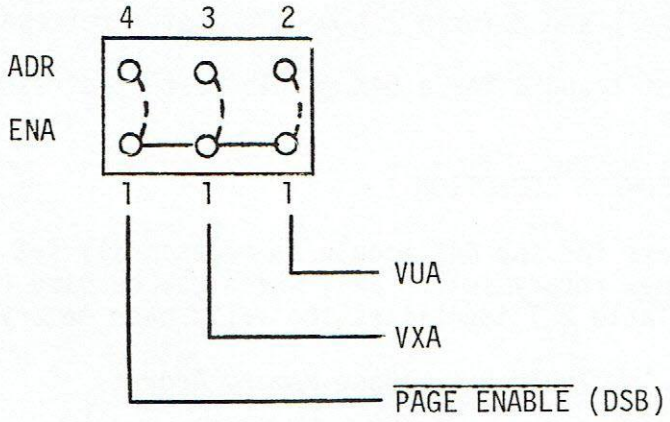
(Select one only)

2.4.2 MEMORY MAP ASSIGNMENT

The user must assign the module to either one of the three map modes:

VUA - Valid User Address
VXA - Valid Executive Address
PAGE ENABLE - For multiple "pages" of 64K bytes

A jumper at ADR ENA is used for this purpose, as illustrated below.



2.4.3 PARITY OPTION

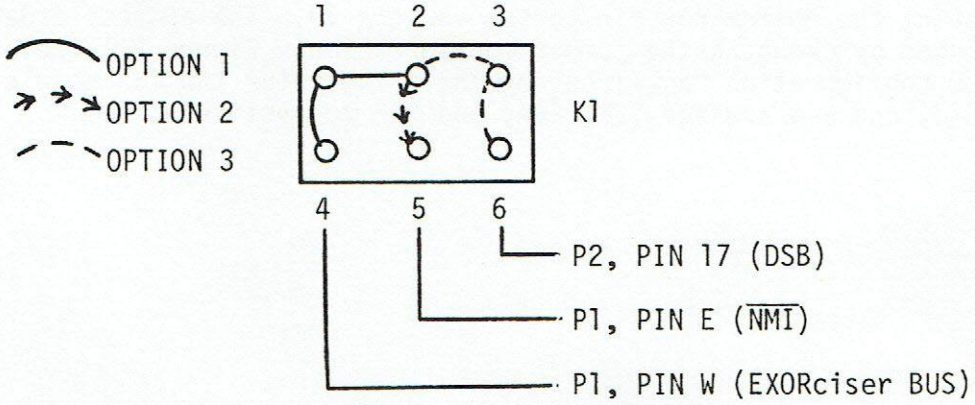
If the user is monitoring parity, he must select one of three options for connecting the parity detect signal to the system. This depends upon the user's system approach to handling parity. Jumper K1 is used to select one of three options.

1. Jumper Pins 1 and 4 to output $\overline{\text{PARITY ERROR}}$ on P1, pin W.

2. Jumper pins 2 and 5 to output $\overline{\text{PARITY ERROR}}$ onto the $\overline{\text{NMI}}$ signal on P1, pin E. In this configuration, the parity error will generate a non-maskable interrupt ($\overline{\text{NMI}}$) for one clock cycle.

3. Jumper pins 2 and 3, and 3 and 6 to output $\overline{\text{PARITY ERROR}}$ on P2, pin 17 (DSB). The usefulness of this configuration depends upon the user's implementation of the Dynamic System Bus.

Jumper K1 is illustrated below.



2.4.4 MASTER/SLAVE REFRESH OPTION

The system may be configured to use one or multiple Dynamic RAM modules. In either case, one module must be configured as a master refresh module and additional modules as slave refresh modules. Jumper K3 is used for this purpose. If no jumper is installed, the module operates as a slave refresh module.

1. Jumper pins 1 and 2 for a 16K module master refresh.

2. Jumper pins 1 and 3 for a 64K module master refresh.

2.4.5 BASE ADDRESS SELECTION

The base address for the 64K module is necessarily set at 0000. The 16K module has a hex rotary switch SW1, which may be used to select one of four 16K blocks. Table 2-1 identifies the valid base memory addresses.

Table 2-1. Base Memory Address

Memory Location	Switch SW1 Position
0000-3FFF	0
4000-7FFF	4
8000-BFFF	8
C000-FFFF	C

2.4.6 DYNAMIC SYSTEM BUS (DSB)

Only two meaningful signals are connected to the Dynamic System Bus connector P2. $\overline{\text{PAGE ENABLE}}$ is connected to P2, pin 19 and $\overline{\text{PARITY ERROR}}$ is connected to P2, pin 17. Pins 18 and 20 are ground.

2.4.7 ADDRESS SELECT HEADER (ADR SEL)

The ADR SEL header is a 20-pin wire-wrap device wired by the factory. These jumpers provide the block (row) address capability. The user can disable specific rows of memory by removing the appropriate jumper and connecting the bottom row pin to top row pin 10. The address order can be rearranged by changing the jumper configuration. Figure 2-1 indicates the ADR SEL configuration "as-wired" by the factory for the 16K module. Figures 2-2, 2-3, and 2-4 are for 32K, 48K, and 64K respectively.

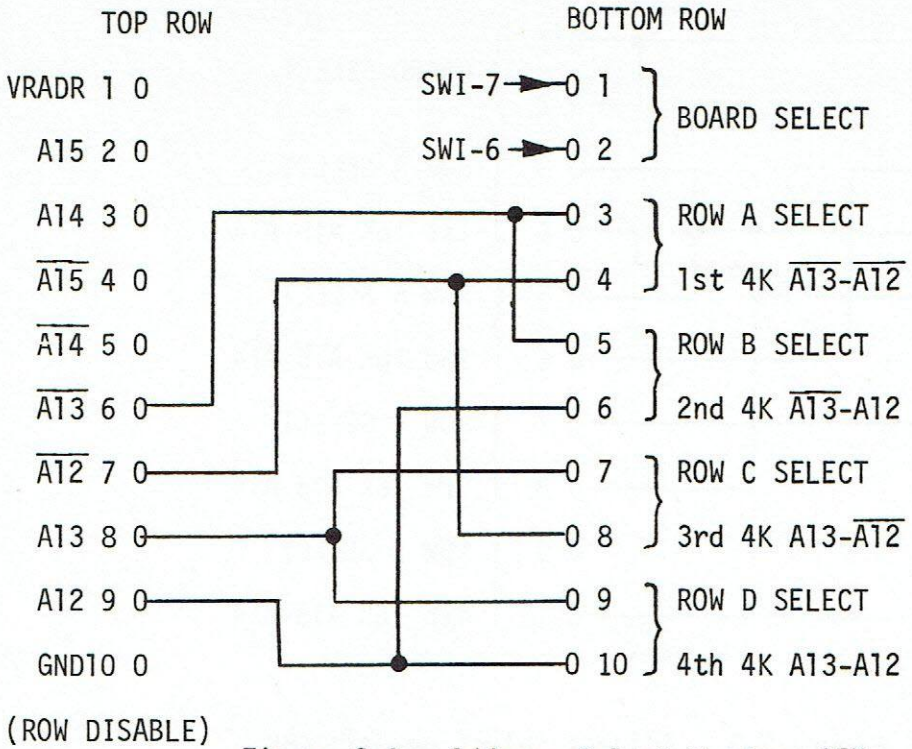


Figure 2-1. Address Select Header, 16K

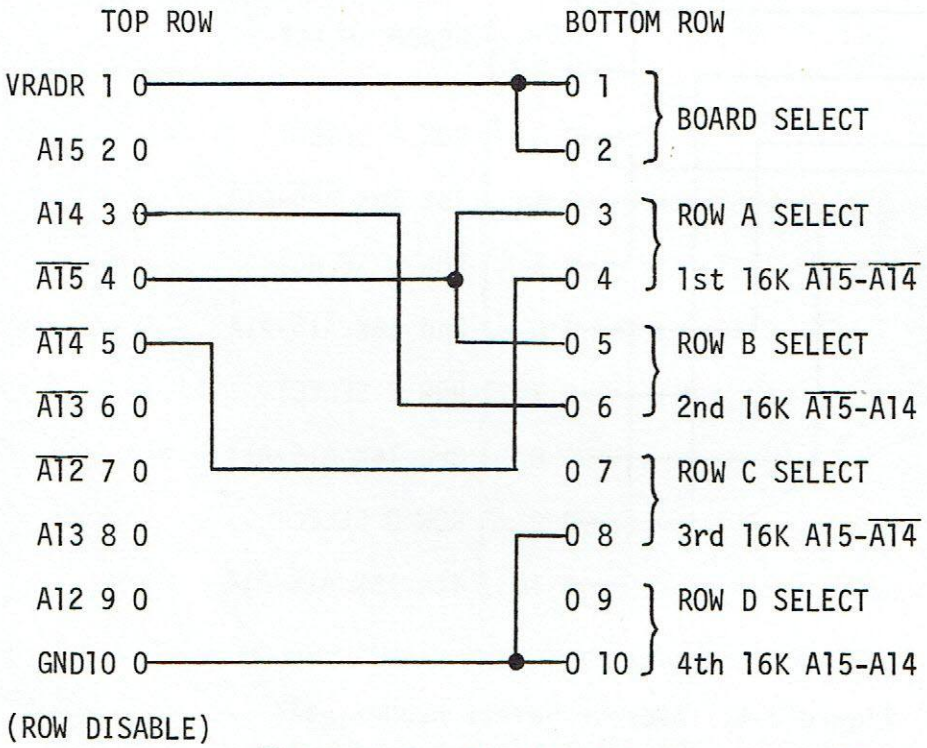


Figure 2-2. Address Select Header, 32K

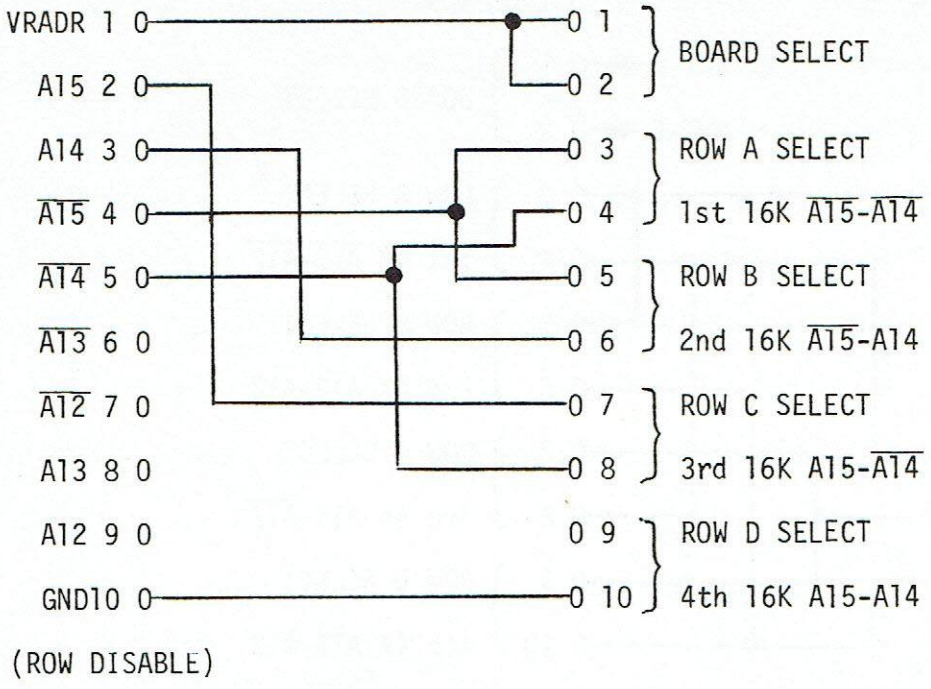


Figure 2-3. Address Select Header, 48K

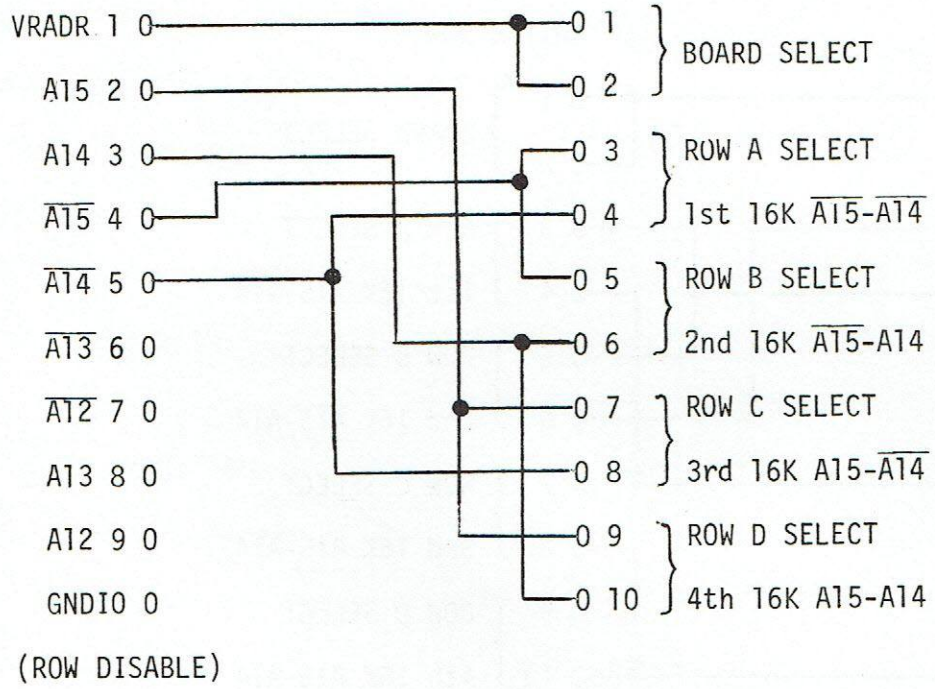


Figure 2-4. Address Select Header, 64K

2.4.8 MISCELLANEOUS JUMPERS

Jumper K5 is factory installed and has no user value.

2.5 INSTALLATION INSTRUCTIONS

Install the Dynamic RAM module as follows:

(a) Turn power OFF on equipment module is being installed in.

CAUTION - INSERTING MODULE WHILE POWER IS APPLIED MAY RESULT IN DAMAGE TO COMPONENTS ON MODULE

(b) Install module in the selected card slot. This module may be installed in any of the 14 card slots in the EXORciser.

(c) Turn power ON.

2.6 MODULE INTERCONNECTIONS

The Dynamic RAM Module interconnects directly with the system bus. The bus signals are identified in Table 2-2. This table lists each pin connection, signal mnemonic, and signal characteristic. Table 2-3 identifies the Dynamic System Bus interface signals on connector P2.

Table 2-2. Connector P1 Bus Interface Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A,B,C,	+5V	+5Vdc - Used by the module logic circuits
D		Not used
E	$\overline{\text{NMI}}$	NON-MASKABLE INTERRUPT
	($\overline{\text{PARITY-ERROR}}$)	(PARITY-ERROR) - This pin is normally the $\overline{\text{NMI}}$ input signal interface. On the Dynamic RAM this pin is an optional $\overline{\text{PARITY-ERROR}}$ output signal interface. When a parity error is detected by the parity check circuitry on the module, the signal will go low causing a non-maskable interrupt to the system.
F-K		Not used
L	MEM CLK	MEMORY CLOCK - This signal is an ungated TTL level OZ clock used to refresh memory in the module.
M	-12V	-12Vdc - Used by the module memory devices

Table 2-2. Connector P1 Bus Interface Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
N-S		Not used
T	+12V	+12Vdc - Used by the module memory devices
U,V		Not used
W	PARITY-ERROR	PARITY ERROR - This pin is an optional PARITY-ERROR output signal interface. This signal line is normally high until a parity error is detected by the parity check circuit on the module at which time the signal will go low for one clock cycle.
X,Y,Z	GND	GROUND
A-F		Not used
H	D3	DATA BUS (bit 3) - One of 8 bidirectional data lines used to provide a two-way data transfer between the Dynamic RAM and any other plug-in modules in the system.
J	D7	DATA bus (bit 7) Same as D3 on P1-H
K	D2	DATA bus (bit 2) Same as D3 on P1-H
L	D6	DATA bus (bit 6) Same as D3 on P1-H
M	A14	ADDRESS bus (bit 14) One of 16 address lines used to select a memory location on this module.
N	A13	ADDRESS bus (bit 13) Same as A14 on P1-M
P	A10	ADDRESS bus (bit 10) Same as A14 on P1-M
R	A9	ADDRESS bus (bit 9) Same as A14 on P1-M
S	A6	ADDRESS bus (bit 6) Same as A14 on P1-M
T	A5	ADDRESS bus (bit 5) Same as A14 on P1-M
U	A2	ADDRESS bus (bit 2) Same as A14 on P1-M
V	A1	ADDRESS bus (bit 1) Same as A14 on P1-M
W,X,Y	GND	GROUND

Table 2-2. Connector P1 Bus Interface Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1,2,3	+5V	+5Vdc - Used by the module logic circuits
4,5		Not used
6	R/W	READ/WRITE - This signal is generated by the MPU and indicates whether the MPU is performing a memory read (high) or write (low) operation. The normal standby state of this signal is read (high). Also, when the MPU is halted, this signal will be in the read state.
7,8,9		Not used
10	VUA	VALID USER'S ADDRESS - This signal, jumper selectable, is produced by the DEbug module. When high, this signal indicates that the address on the address bus is valid and the MPU is NOT addressing the EXbug program.
11	-12V	-12Vdc - Used by the module memory devices
12	$\overline{\text{REF-REQ}}$	REFRESH REQUEST - This input signal to the MPU module, when low, initiates a memory refresh cycle of Dynamic RAM module. During the refresh operation, the clock is inhibited from generating the Ø1 (held high) and Ø2 (held low) clock signals. However, during the refresh operation, the MEM CLK signal is still generated in order to provide the necessary refresh clock.
13	REF-GRANT	REFRESH GRANT - This output signal from the MPU module, when high, instructs the Dynamic RAM modules to refresh their memories.
14, 15		Not used
16	+12V	+12Vdc - Used by the module memory devices
17, 18		Not used
19	VXA	VALID EXECUTIVE ADDRESS - A high level signal, jumper selectable, generated by the DEbug module in place of the VUA signal when the system is operating in the Dual Map Mode and the EXbug Program is addressing the Executive portion of the memory map.

Table 2-2. Connector P1 Bus Interface Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
20,21,22	GND	GROUND
29	$\overline{D1}$	DATA bus (bit 1) Same as on P1-$\overline{H}$
30	$\overline{D5}$	DATA bus (bit 5) Same as $\overline{D3}$ on P1-$\overline{H}$
31	$\overline{D0}$	DATA bus (bit 0) Same as $\overline{D3}$ on P1-$\overline{H}$
32	$\overline{D4}$	DATA bus (bit 4) Same as $\overline{D3}$ on P1-$\overline{H}$
33	A15	ADDRESS bus (bit 15) Same as A14 on P1-$\overline{M}$
34	A12	ADDRESS bus (bit 12) Same as A14 on P1-$\overline{M}$
35	A11	ADDRESS bus (bit 11) Same as A14 on P1-$\overline{M}$
36	A8	ADDRESS bus (bit 8) Same as A14 on P1-$\overline{M}$
37	A7	ADDRESS bus (bit 7) Same as A14 on P1-$\overline{M}$
38	A4	ADDRESS bus (bit 4) Same as A14 on P1-$\overline{M}$
39	A3	ADDRESS bus (bit 3) Same as A14 on P1-$\overline{M}$
40	A0	ADDRESS bus (bit 0) Same as A14 on P1-$\overline{M}$
41,42,43	GND	GROUND

Table 2-3. Connector P2 Dynamic System Bus

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
17	$\overline{\text{PARITY-ERROR}}$	PARITY ERROR - Same as PARITY ERROR on P1-W. Jumper selectable.
18	GND	GROUND
19	$\overline{\text{PAGE ENA}}$	PAGE ENABLE - If a user builds a controller that can convert the VMA signal from the MPU into one of several pages, an unlimited number of "pages" of 64K bytes can be realized. This signal port is jumper selectable.
20	GND	GROUND

CHAPTER 3

THEORY OF OPERATION

3.1 INTRODUCTION

This chapter provides a block diagram description of the Dynamic RAM Module. The block diagram is shown in Figure 3-2. A schematic diagram is shown in Figure 3-3.

3.2 BLOCK DIAGRAM DESCRIPTION

The Dynamic RAM Module receives the 16 address lines A0 to A15, a MEM-CLK (Memory Clock) timing signal, VUA (Valid User's Address), VXA (Valid Executive Address), and PAGE-ENA (Page Enable) signals for address MAP Control. Also received are the R/W (read/write) line and a high going level REF-GNT (Refresh Grant) signal during each memory operation. In addition, during a memory read operation, this module also receives the eight data bits $\overline{D0}$ through $\overline{D7}$ from the MPU.

During a memory operation, the module first applies A0-A5 (16K) or A0-A6 (64K) called Row address to the memory array out of an address multiplexer, followed by A6-A11 (16K) or A7-A13 (64K) called Column address. This multiplexing allows access to the large amounts of locations contained within one memory device. During a refresh cycle, the multiplexer outputs a special refresh Row address only, incrementing the special address after each refresh cycle is completed.

The module address bus interface, upon receiving the Memory Clock signal, generates ℄RAS (Row Address Select) signal from the module's control logic, which latches the 16 system address bits for use throughout the subsequent cycle. The address interface applies the four address bits A12 through A15 and their complements to address decoding logic in a manner dependent upon the 16K or 64K basic board configuration. The board's internal address bus also time multiplexes the 12 (16K) or 14 (64K) address lines to the memory array. The first group of addresses (ADR-0 to 5 or ADR-0 to 6) are latched into the memory devices when the $\overline{RAS}$ (Row address select) line falls. The 2nd half of the multiplexed address lines are then placed on the memory array address lines and the CAS (Column address select) latches these into the device.

During a write cycle (depending on the system speed),a write pulse is generated to write the data coming in from the MPU to the addressed memory array location. Approximately 200ns after the devices are addressed during a read, data is present at the output of the module.

Figure 3-1 shows the module's timing relationships with nominal times indicated.

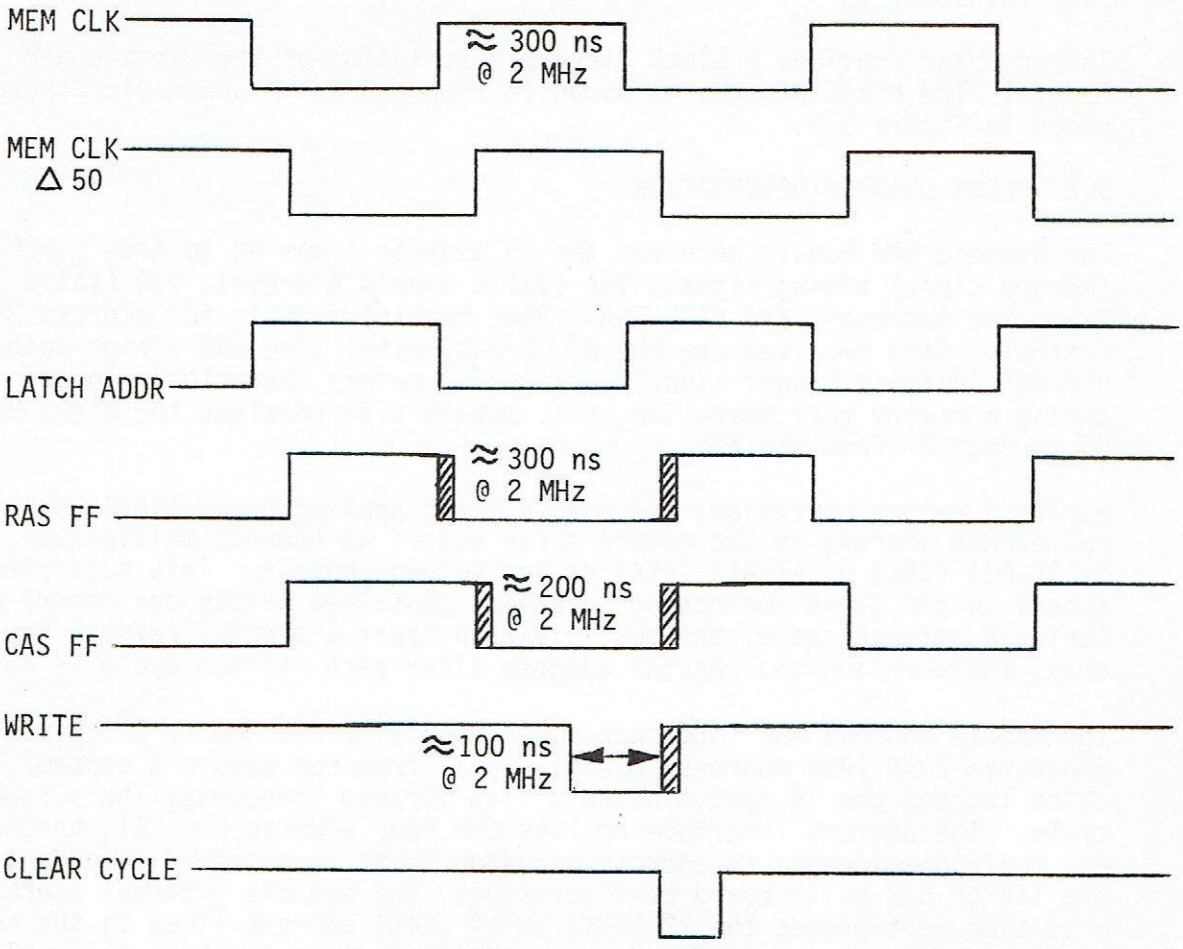


Figure 3-1. Timing Diagram

The system Memory Clock is the timing reference signal for the board. The RAS and CAS signals are derived from the module control logic. The ØRAS signal is started at the leading edge of Memory Clock, but delayed by other logic circuits. The CAS signal is generated approximately 60ns after the rising edge of Memory Clock. Both signals end when the Memory Clock signal goes low. These two signals are frequency independent up to 2 MHz (the maximum operation rate).

The write pulse to the memory array during a MPU write cycle is frequency dependent and is controlled by a 9602 one shot, RC time constant. The write clock begins sufficiently far into the cycle to guarantee data from the MPU. Three speed ranges of write clock, jumper selected, at K2 are available; 1.0, 1.5 and 2.0.

The address multiplexer MSI 3242 serves a dual function. It is responsible for the address multiplexing for the Row and Column address, as well as the refresh counter address output.

The normal output of this 3242 circuit is the Row address, except during a refresh cycle. During this time, the refresh counter contents are output. Forty nanoseconds into a memory cycle, the output of the multiplexer is changed to the column address; this remains for the remainder of the cycle.

The ADR-6 output of the 3242 circuit has two jumper options at K5 (see schematic). The 16K option (3 to 4) places refresh grant on the chip select input to the 4KX1 dynamic devices. Since this is a low true signal, the devices are enabled at all times

When K5 is patched from Pin 1 to 2, the ADR-6 line is patched through to the 16KX1 devices which require the additional multiplexed address line.

The data bus interface provides a two-way transfer between the RAM memory array and the EXORciser bus. The parity circuit monitors the array's input and output data. The driver circuits in the data bus interface are three-state devices whose operation is controlled by the control logic. These devices, in their disabled or off state, provide high outputs to their respective buses.

The parity circuit monitors the data being transferred between the RAM memory array and the data bus and can indicate a parity error on three patchable lines.

The Dynamic RAM Module is supplied with the even parity logic. As data is written to the module, an even bit is generated and stored with the data byte. As data is read out of the module, the byte is checked against the parity bit. A parity error, when detected, is optionally sent to either the EXORciser bus interface or to the Dynamic System Bus (DSB).

The memory array is organized into four rows by nine columns of either 4KX1 or 16KX1 dynamic memory devices. The address bits A12 and A13 (16K module) or A15 and A14 (64K module) select the row of devices to be read - row A, B, C, or D. The MCM4027 devices are organized into a 64 by 64 array and require 12 address lines. The MCM6616 devices are organized into a 128 by 128 array and require 14 address lines. By time multiplexing the addresses for the rows (6 address lines for 16K, 7 address lines for 64K) and columns, the devices only require one half of the address lines at one time. In addressing these devices, the module decodes A12, A13, or A14, A15 to determine which of the four rows of devices is to be read.

The refresh grant input to the memory module is a result of a regular, periodic REFRESH-REQUEST signal generated on the module. The System MPU board initiates the REF Grant signal during a period when all other system activity is halted.

The multiplexer logic responds to the Refresh Grant by enabling the refresh row address out to the devices, inhibiting a CAS and generating a RAS. When the REF Grant signal goes away,the refresh address is no longer enabled and the multiplexer internal refresh counter is incremented.

The address from the MPU is latched at the beginning of each Memory Clock. Since these latches are "fall through", the true input appears at the output before being latched. The output of these latches goes to both address decoding logic and the address multiplexer. The address decoding logic determines if the board is being addressed. If the board is being selected, the logic creates the gating necessary to generate a ¢RAS for the appropriate row of devices in the memory array. If the cycle is a MPU read this decode also creates the signal which turns on the module output buffers.

The RAS and first 6 or 7 address lines are cycled to the memory devices first, followed by a CAS and the next 6 or 7 address lines. This timing is discussed earlier in this guide.

The read and write operation on this board differ only by the level of the read/write line. A high on this line indicates a read, while a low indicates a write. The low signal activates the write flip-flop and causes data to be enabled into the board, so that it may be written. The read indication does not enable the write flip-flop, but enables the data out of the board. All other module timing remains the same.

Through a jumper connection at K3, the Dynamic RAM Module may be configured to function as a "master" or "slave" refresh module. When the module is configured as a 16K RAM, it must be refreshed every 32 µsec and K3 must be jumpered from 1 to 2. When the module is configured as a 64K module, it must be refreshed every 15 µsec and K3 must be jumpered from 1 to 3. Neither jumper should be connected if the board is to be used as a slave.

The ADR SEL header is configured so that Row A is 00, B is 01, C is 10, and D is 11 in terms of combinations of A12, 13 or A14, 15, depending on whether the board is a 16 or 64K configuration.

The 32K and 48K versions of the module have the enables removed from the RASD, RASC logic (in that order); one for each 16K size deleted. Grounding an input to one of the control inputs to each Row select guarantees that address block will not be selected.

The ADR-ENA header has provisions for connecting VUS, VXA, or PAGE-ENA to the board enable logic, depending on the application the module must fit.

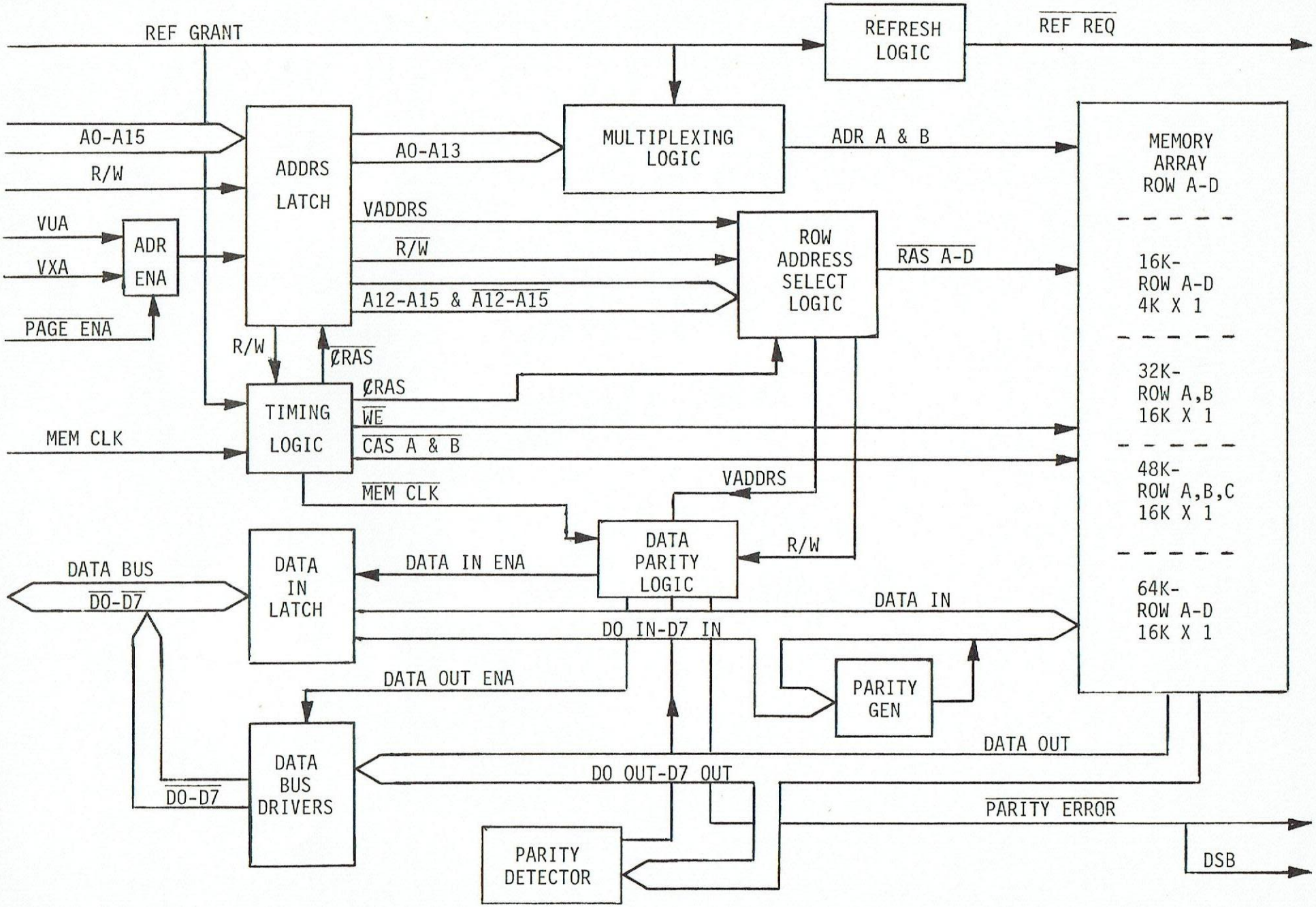
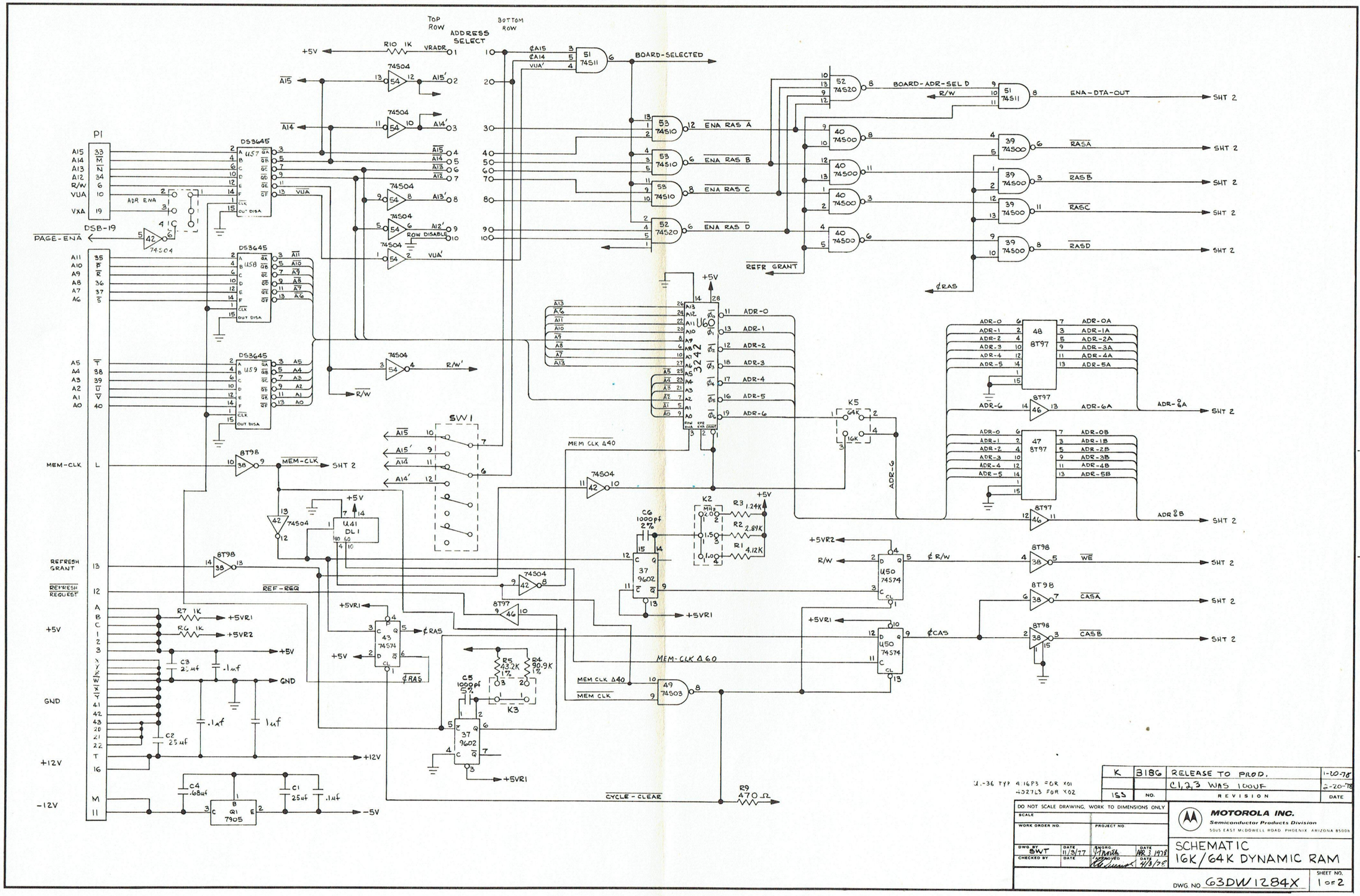


FIGURE 3-2. Dynamic RAM Block Diagram



K	3186	RELEASE TO PROD.	1-20-78
		C1,2,3 WAS 100UF	2-20-78
ISS	NO.	REVISION	DATE

U1-36 TYP 4116P3 FOR X01
4027L3 FOR X02

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SCHEMATIC
16K/64K DYNAMIC RAM

DWG NO. 63DW1284X

SHEET NO. 1 OF 2

FIGURE 3-3. Dynamic RAM Schematic Diagram (Sheet 1)

BOARD POPULATION TABLE - MEMORY ARRAY

ASSY	01DW1284X01	DEVICES IN	U1-U36
	01DW1284X02	DEVICES IN	U1-U36
	01DW1284X03	DEVICES IN	U1-U18, 19, 21, 23, 25, 27, 29, 31, 33, 35
	01DW1284X04	DEVICES IN	U1-U18

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SCHEMATIC DIAGRAM
16K/64K DYNAMIC RAM

DWG. NO. 63DW1284X | SHEET NO. 2 OF 2

Figure 3-3. Dynamic RAM Schematic Diagram (Sheet 2)

CHAPTER 4

PARTS

4.1 INTRODUCTION

This chapter provides the parts list for the Dynamic RAM Modules. The list reflects the latest issue of the hardware at the time of printing. Parts locations are shown on Figure 4-1.

Table 4-1. Dynamic RAM Modules Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION	EFFEC-TIVITY
	84DW6284x01	Printed Wiring Board Dynamic RAM	L
	55NW9403A10	Ejector, Circuit Card with Roll Pin Attachment, 2 required	K
C1,C2,C3	23NW9618A33	Capacitor, Electrolytic, 25 MFD @ 16VDC	K
C4	21NW9604A18	Capacitor, Fixed, Ceramic, 0.68 MFD @ 50VDC	K
C5	21NW9605A12	Capacitor, Fixed, Mica, 1000 PF @ 100 VDC	K
C6	21NW9605A13	Capacitor, Fixed, Mica, 100 PF @ 500 VDC	K
C7-C14,C16, C18,C20,C22, C24,C28,C30, C32,C34,C36, C38,C40,C42, C44,C46,C48, C50,C52,C54, C56,C58,C60, C62,C64,C66, C68,C70,C72, C74,C76,C78, C80,C82,C84, C86,C87-C107	21NW9702A09	Capacitor, Fixed, Ceramic, 0.1 MFD @ 50 VDC (64 required for 16K and 64K modules only)	K
C7-C14,C16, C18,C20,C22, C24,C28,C30, C32,C34,C36, C38,C40,C42, C44,C46,C48, C50,C87-C107	21NW9702A09	Capacitor, Fixed, Ceramic, 0.1 MFD @ 50 VDC (46 required for 32K module only)	K

Table 4-1. Dynamic RAM Modules Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION	EFFEC-TIVITY
C7-C14,C16, C18,C20,C22, C24,C28,C30, C32,C34,C36, C38,C40,C42, C44,C46,C48, C50,C52,C56, C60,C64,C68, C72,C76,C80, C84,C87-C107	21NW9702A09	Capacitor, Fixed, Ceramic 0.1 MFD @ 50 VDC (55 required for 48K module only)	K
C15,C17,C19, C21,C23,C25, C27,C29,C31, C33,C35,C37, C39,C41,C43, C45,C47,C49, C51,C53,C55, C57,C59,C61, C63,C65,C67, C69,C71,C73, C75,C77,C79, C81,C83,C85	21NW9604A08	Capacitor, Fixed, Ceramic, 1.0 MFD @ 50 VDC (36 required for 16K and 64K modules only)	K
C15,C17,C19, C21,C23,C25, C27,C29,C31, C33,C35,C37, C39,C41,C43, C45,C47,C49	21NW9604A08	Capacitor, Fixed, Ceramic, 1.0MFD @ 50 VDC (18 required for 32K module only)	K
C15,C17,C19, C21,C23,C25, C27,C29,C31, C33,C35,C37, C39,C41,C43, C45,C47,C49, C51,C55,C59, C63,C67,C71, C75,C79,C83	21NW9604A08	Capacitor, Fixed, Ceramic, 1.0 MFD @ 50 VDC (27 required for 48K module only)	K
K1,K2,ADR ENA	28NW9802B88	Header, Double Row Post, 6 Pin	K
K3	29NW9805A46	Terminal, Wire-Wrap, Feed-Thru, .025 square	K
K5	28NW9802C29	Header, Double Row Post, 4 pin	K

Table 4-1. Dynamic RAM Modules Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION	EFFEC-TIVITY
P2,ADR SEL	28NW9802C12	Header, Double Row Post, 20 Pin	K
Q1	51NW9615C39	Voltage Regulator MC7905CT	K
R1	06NW9602A41	Resistor, Fixed, Film, 4.12K OHM, 1%, 1/4 W	K
R2	06NW9602A70	Resistor, Fixed, Film, 2.87K OHM, 1%, 1/4 W	K
R3	06NW9602A69	Resistor, Fixed, Film, 1.24K OHM, 1%, 1/4 W	K
R4	06NW9602A19	Resistor, Fixed, Film, 90.0K OHM, 1%, 1/4 W	K
R5	06NW9602A71	Resistor, Fixed, Film 43.2K OHM, 1%, 1/4W	K
R6,R7,R10	06SW-124A49	Resistor, Fixed, Carbon, 1K OHM, 5%, 1/4 W	K
R8	06SW-124A65	Resistor, Fixed, Carbon, 4.7K OHM, 5%, 1/4 W	K
R9, R11	06SW-124A41	Resistor, Fixed, Carbon, 470 OHM, 5%, 1/4 W	K
S1	40NW9801A31	Switch, Hex, 53137-1 (16K module only)	K
U1-U36	51NW9615E36	I.C. MCM4027L3 (16K Module only)	K
U1-U18	51NW9615E37	I.C. MCM4116C20 (32K Module only)	K
U1-U18,U19, U21,U23,U25, U27,U29,U31, U33,U35	51NW9615E37	I.C. MCM4116C20 (48K Module only)	K
U1-U36	51NW9615E37	I.C. MCM4116C20 (64K Module only)	K
U37	51NW9615E31	I.C. DM9602N	K
U38	51NW9615C36	I.C. 8T98	K
U39, U4	51NW9615C94	I.C. SN74SDON	K
U41	01NW9804B35	Module, Digital Delay, 100ns	K

Table 4-1. Dynamic RAM Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION	EFFEC-TIVITY
U42, U54	51NW9615C96	I.C. SN74S04N	K
U43, U50	51NW9615C95	I.C. SN74S74N	K
U44, U45	51NW9615F19	I.C. 8T26A	K
U46,U47,U48	51NW9615B71	I.C. 8T97 (16K, 48K, and 64K Modules only	K
U46, U48	51NW9615B71	I.C. 8T97 (32K Module only)	K
U49	51NW9615E33	I.C. 74S03A	K
U51	51NW9615D90	I.C. SN74S11N	K
U52	51NW9615D92	I.C. SN74S20N	K
U53	51NW9615E	I.C. 74S10A	K
U55, U56	51NW9615F12	I.C. SN74LS280	K
U57,U58,U59	51NW9615E32	I.C. DS3645N	K
U60	51NW9615E30	I.C. 3242	K
	28NW9802B07	Socket, I.C., 16 Pin (36 required for 16K and 64K, 18 required for 32K, 27 required for 48K Mdoules)	K
	43NW9002A52	Bushing, Insulator (use with Q1)	K
	29NW9805A91	Jumper, 2 position (use at K2)	K

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